UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,572	09/15/2003	Philip Yeung	9797-0139-999	2981

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EXAMINER
WALLING, MEAGAN S

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/663,572	YEUNG, PHILIP
	Examiner	Art Unit	
	Meagan S. Walling	2863	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 May 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 17-20, 28-30 and 32* is/are rejected.

7)☒ Claim(s) *15, 16, 21-27 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1.   Claims 1-5, 13, 17-21, 28-30, and 32 are rejected under 35 U.S.C. 102(e) as being

anticipated by Coyle et al. (US 6,609,221).

Regarding claim 1, Coyle et al. teaches loading a first pattern into a controller pattern

buffer (416) of a controller (404 and column 13, lines 53-55); transmitting the first pattern to a

component of the components (column 13, lines 55-57); capturing the transmitted first pattern in

a component capture buffer (436) of the component (column 13, lines 58-61); performing at the

controller a first comparison to compare the captured first pattern to the first pattern (column 13,

lines 63-64); and identifying any interconnect faults based on the first comparison (column 13,

lines 64-65).

Regarding claim 2, Coyle et al. teaches preparing the component capture buffer to

capture the transmitted first pattern (column 4, lines 1-5 and Ref. 504).

Regarding claim 3, Coyle et al. teaches placing the component in an interconnect test

mode (column 4, lines 1-5 and Ref. 504).

Regarding claim 4, Coyle teaches that the component is a memory device (column 5, line

35).

Regarding claim 5, Coyle et al. teaches transferring the captured first pattern from the component capture buffer to the controller (column 9, lines 56-60).

Regarding claim 13, Coyle et al. teaches loading a second pattern into a component pattern buffer of the component (column 10, line 29); transmitting the second pattern to the controller (column 10, lines 34-36); capturing the transmitted second pattern in a controller capture buffer of the controller (416); and performing a second comparison to compare the captured second pattern to the second pattern, wherein the step of identifying any interconnect faults is based on the first comparison and the second comparison (column 10, lines 51-55).

Regarding claim 17, Coyle et al. teaches that the second pattern is identical to the first pattern (column 10, line 31).

Regarding claim 18, Coyle et al. teaches a first component (222) comprising first core circuitry (402), first interface circuitry (406), a pattern buffer configured to store a pattern (438), and a first communication path coupling the first core circuitry to the first interface circuitry (see Fig. 4A); a second component (224) comprising second core circuitry (222), second interface circuitry (406), and a second communication path coupling the second core circuitry to the second interface circuitry (see Fig. 4A), and interconnect circuitry (401) coupling the first component to the second component, wherein a capture buffer is coupled to the first communication path for capturing the pattern transmitted by the first component as a captured pattern (436); and a link between the second component and the first component, where the link is configured to transfer the captured pattern from the second component to the first component for comparison with the pattern (column 6, lines 15-17 and Ref. 205).

Regarding claim 19, Coyle et al. teaches that the second capture buffer is coupled to the

second communication path (438).

Regarding claim 20, Coyle et al. teaches that the communication path comprises a first

transmit and receive path (205), wherein the first capture buffer comprises a first transmit

capture buffer (438) coupled to the first transmit communication path and a first receive buffer

coupled to the first receive communication path (436).

Regarding claim 28, Coyle et al. teaches a memory controller (404) comprising a

controller pattern buffer (416) configured to store a pattern; and a memory device coupled to the

memory controller, wherein the memory controller comprises core circuitry (402), interface

circuitry, and a communication path coupling the core circuitry to the interface circuitry (see Fig.

4A), wherein a capture buffer (436) is coupled to the communication path for capturing the

pattern transmitted by the memory controller as a captured pattern; and a link between the

memory device and the memory controller, where the link is configured to transfer the captured

pattern from the memory to the memory controller for comparison with the pattern (see Fig. 4A).

Regarding claim 29, Coyle et al. teaches a transmit communication path (434) and a

receive communication path (432), wherein the capture buffer comprises a transmit capture

buffer (438) coupled to the transmit communication path and a receive capture buffer (436)

coupled to the receive communication path.

Regarding claim 30, Coyle et al. teaches a multiplexer configured to select between a first

input coupled to the core circuitry and a second input coupled to a pattern buffer (444).

Regarding claim 32, Coyle et al. teaches a first component (222) comprising first core

circuitry (402), first interface circuitry (406), a means for storing a test pattern (438), and a first

communication means for coupling the first core circuitry to the first interface circuitry (see Fig.

4A); a second component (224) comprising second core circuitry (222), second interface

circuitry (406), and a second communication means for coupling the core circuitry to the

interface circuitry (see Fig. 4A), and interconnection means (401) for coupling the first

component to the second component, wherein a means for capturing the test pattern received

from the first component is coupled to the first communication means (436); and a link between

the second component and the first component, where the link is configured to transfer the

captured pattern from the second component to the first component for comparison with the test

pattern (column 6, lines 15-17 and Ref. 205).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   Claims 6-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle

et al. in view of Mak et al. (US 6,885,209).

Regarding claim 7, Coyle et al. teaches that the step of transmitting the first pattern is

performed via control bus (column 2, lines 25-27).

Regarding claim 8, Coyle et al. teaches loading a second pattern into the memory device

(column 10, line 29); performing a memory read operation (column 10, lines 33-34); capturing

the second pattern received from the memory device (column10, lines 39-40); performing a

second comparison to compare the capture second pattern to the second pattern (column 10, lines

51-55); and identifying any interconnect faults based on the second comparison (column 10,

lines 51-55).

Regarding claim 9, Coyle et al. teaches that the step of performing the memory read

operation is performed via a control bus (column 2, lines 25-27).

Regarding claim 10, Coyle et al. teaches that the step of capturing the second pattern is

performed by capturing the second pattern received from the memory device via a data bus

(column 2, lines 25-27).

Regarding claim 11, Coyle et al. teaches loading the second pattern into the controller

pattern buffer of the controller (column 10, lines 35-37).

Regarding claim 12, Coyle et al. teaches that the second pattern is identical to the first

pattern (column 10, line 31).

Coyle et al. teaches all of the limitations of claims 6, 8, and 14 except the limitation that

the step of transferring the capture first pattern, loading the first and second patterns is performed

via serial link.

Mak et al. teaches transferring and loading patterns via serial link (column 4, lines 50-

54).

It would have been obvious at the time of the invention to combine the teachings of

Coyle et al. with the teachings of Mak et al. to transfer and load patterns using a serial link. The

motivation for making this combination would be to transfer and load patterns quickly and

efficiently.

Allowable Subject Matter

3.   Claims 15, 16, 21-27, and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the indication of allowability of claim 15 is the inclusion of the limitation that the step of loading the second pattern is performed by loading a stored pattern from an embedded memory element of the component. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 16 is the inclusion of the limitation that the component is a graphics processor. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 21 is the inclusion of the limitation of a second transmit communication path and a second receive communication path, wherein the second capture buffer further comprises a second transmit capture buffer coupled to the second transmit communication path and a second receive capture buffer coupled to the second receive communication path. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 31 is the inclusion of the

limitation that the memory device is coupled to the memory controller via a memory serial link,

a control bus, and a data bus. It is this limitation in the claimed combination that has not been

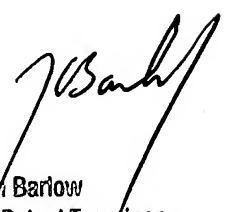found, taught, or suggested by the prior art that makes these claims allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283.

The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

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